What is claimed is:

1. A decoder circuit comprising:

a plurality of output nodes;

a charge sharing node;

a charge sharing enable generator adapted to assert a charge sharing enable signal when an address changes; and

a plurality of switching devices coupled to be responsive to the charge sharing enable signal, wherein the plurality of switching devices are adapted to conditionally couple two of the plurality of output nodes to the charge sharing node concurrently.

2. The decoder circuit of claim 1 further comprising a charge recycling control circuit coupled to receive the charge sharing enable signal and produce a control signal to control one of the plurality of switching devices.

3. The decoder circuit of claim 2 wherein the charge recycling control circuit includes a tri-state driver adapted to conditionally drive one of the plurality of output nodes.

4. The decoder circuit of claim 3 wherein the tri-state driver includes an inverter having two additional transistors adapted to be turned off at the same time.

5. The decoder circuit of claim 1 wherein the charge sharing enable generator includes a programmable delay element to influence a width of the charge sharing enable signal.

6. The decoder circuit of claim 1 wherein the charge sharing enable generator includes a fixed delay element to influence a width of the charge sharing enable signal.

7. The decoder circuit of claim 1 wherein the plurality of switching devices comprise PMOS transistors.

8. The decoder circuit of claim 1 wherein the plurality of switching devices consists of PMOS transistors.

9. A decoder circuit comprising:

a charge sharing enable generator adapted to produce a charge sharing enable signal having a programmable width when an address changes;

a first charge recycling control circuit coupled between the charge sharing enable generator and a first output node;

a second charge recycling control circuit coupled between the charge sharing enable generator and a second output node;

a first switching device responsive to the first charge recycling control circuit coupled between a charge sharing node and the first output node; and

a second switching device responsive to the second charge recycling control circuit coupled between the charge sharing node and the second output node.

10. The decoder circuit of claim 9 wherein the charge sharing enable generator includes a state machine adapted to detect a change in the address.

11. The decoder circuit of claim 9 wherein the first charge recycling control circuit comprises a tri-state driver adapted to conditionally drive the first output node.

12. The decoder circuit of claim 11 wherein the tri-state driver comprises:

two transistors coupled to form an inverter; and

two transistors adapted to turn off when the first switching device is on.

13. The decoder circuit of claim 9 wherein the first charge recycling control circuit comprises a sequential element to detect whether the first output node will change state.

14. An electronic system comprising:

a receiver adapted to receive communications signals;

a processor coupled to the receiver; and

a memory coupled to the processor, the memory having a decoder circuit that includes:

a plurality of output nodes;

a charge sharing node;

a charge sharing enable generator adapted to assert a charge sharing enable signal when an address changes; and

a plurality of switching devices responsive to the charge sharing enable signal, wherein the plurality of switching devices are adapted to conditionally couple two of the plurality of output nodes to the charge sharing node concurrently.

15. The electronic system of claim 14 wherein the decoder circuit further comprises a charge recycling control circuit coupled to receive the charge sharing enable signal and produce a control signal to control one of the plurality of switching devices.

16. The electronic system of claim 15 wherein the charge recycling control circuit includes a tri-state driver adapted to drive one of the plurality of output nodes.

17. The electronic system of claim 16 wherein the tri-state driver includes an inverter having two additional transistors adapted to be turned off at the same time.

18. The electronic system of claim 14 wherein the charge sharing enable generator includes a programmable delay element to influence a width of the charge sharing enable signal.

19. The electronic system of claim 14 wherein the charge sharing enable generator includes a fixed delay element to influence a width of the charge sharing enable signal.

20. A method comprising:

decoding a first address;

generating a charge sharing enable signal when the address changes from the first address to a second address;

decoding the second address; and

sharing charge between a first decoder output node corresponding to the first address and a second decoder output node corresponding to the second address.

21. The method of claim 20 wherein generating a charge sharing enable signal comprises specifying a width of the charge sharing enable signal.

22. The method of claim 21 wherein specifying a width comprises setting a value of a programmable delay element.

23. The method of claim 20 wherein sharing charge comprises tri-stating a first output driver adapted to conditionally drive the first decoder output node.

24. The method of claim 23 wherein sharing charge further comprises tri-stating a second output driver adapted to conditionally drive the second decoder output node.

25. The method of claim 24 wherein sharing charge further comprises coupling the first and second decoder output nodes together.